New Millennium Program Office
Microelectronics Systems

The New Millennium Program

Towards a Spacecraft on a Chip

Leon Alkalai
Jet Propulsion Laboratory
tel. 818 354 5988
email: leon@cs.jpl.nasa.gov

Outline:

1. A Historic Perspective
2. A Vision for the New Millennium
3. Integrated Product Development Team (IPDT) Technology Roadmap
   - 3D VLSI Architecture Technology Development
   - Low Power Electronics Technology Development
4. Deep-Space 1 and 2 Avionics Architectures
5. Customers and Partners

New Millennium Program Office
Microelectronics Systems

A Historic Perspective

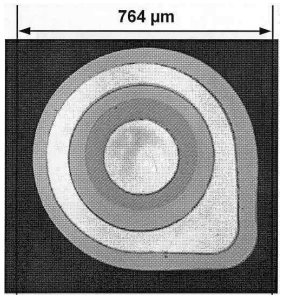
New Millennium Program Office
Microelectronics Systems

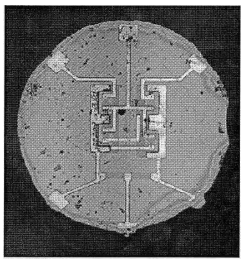
N M P

A Historic Perspective

Transistor — Integrated Circuit — Intel 4004 µP — Pentium Pro P6

40s - 50s **1961** **1971** **1996**





2.3 K Tr. — 5.5 M Tr.

25,000 x improvement in performance;
1000 x rise in cost of development.

Source: Intel

A Historic Perspective

Perhaps more than any other single technology of the 20th century, semiconductor microelectronics technology has transformed almost every aspect of modern society:

- Information Technologies
- Transportation
- Communication
- Science and Education
- Medicine
- Design, automation, and manufacturing
- Entertainment

New Millennium Program Office
Microelectronics Systems

N M P

A Historic Perspective

Stone Age

Bronze Age

3000 BCE
East Anatolia

1000 BCE
Middle East

Iron Age

Middle East, Europe

Silicon Age

Stone, Bronze, Iron, Silicon Age

1948
Silicon Valley, USA

New Millennium Program Office
Microelectronics Systems

A Vision for the New Millennium

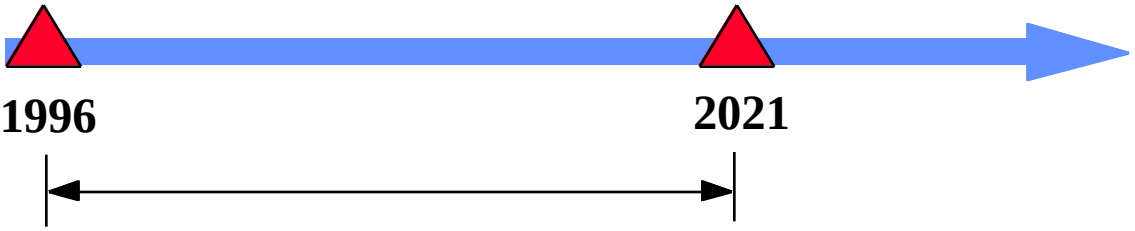
Vision: The Next 25 years

"Every 18 months microprocessors double in speed. Within 25 years, one computer will be as powerful as all those in the Silicon Valley."

David A. Patterson
Professor, UC Berkeley
Scientific American
September 1995

Vision: The Next 25 years

Pentium Pro
P6



1996 **2021**

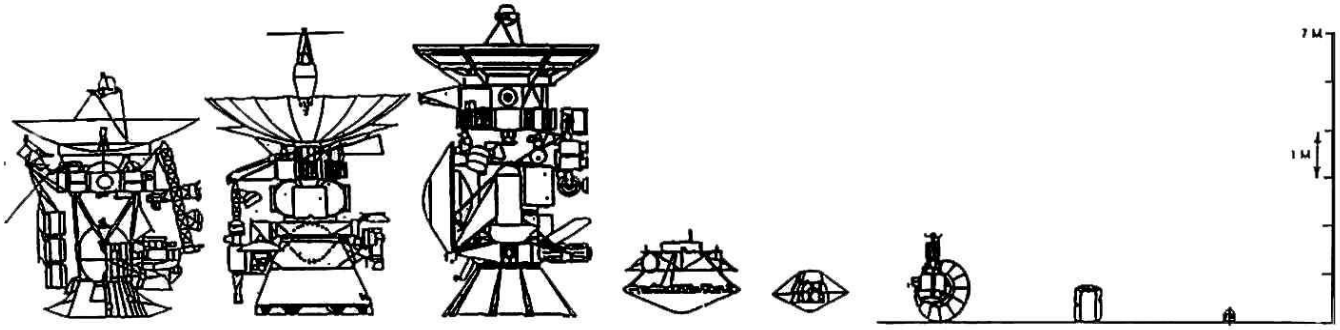
5.5 M Tr.

- System on a Chip
- Low-Power Electronics
- 3D VLSI Electronics
- Continued Performance Growth

New Millennium Program Office
Microelectronics Systems

N M P

Towards the Second Generation Spacecraft

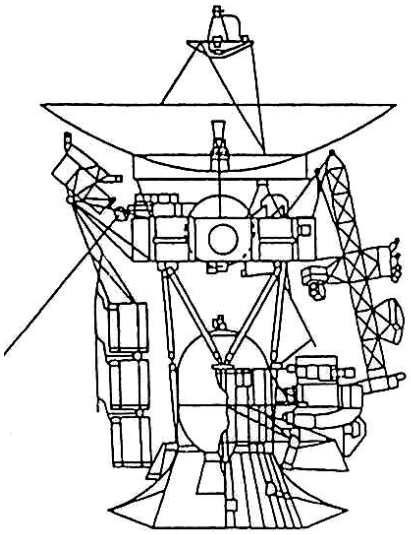


Voyager	Galileo	Cassini	Pathfinder	Mini-Geo	Pluto	Acme-3	2nd Gen μS/C
1976	1989	1997	1996	1998	2000	2002	2005

New Millennium Program Office
Microelectronics Systems

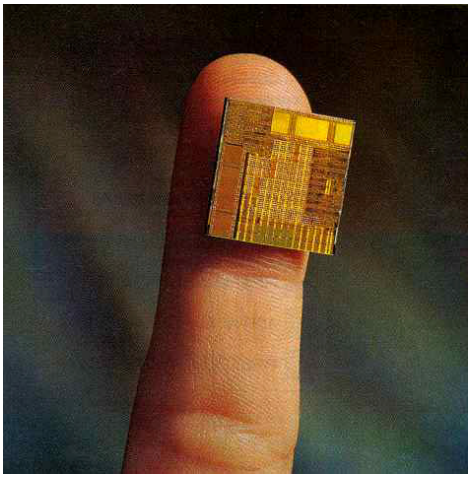
N M P

Vision: A Spacecraft on a Chip



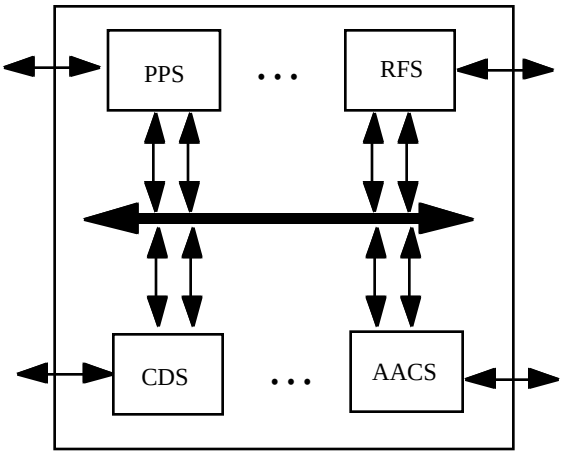
VOYAGER
VOLUME = 62 m^3
MASS (DRY) = 986 kg
POWER = 430 W

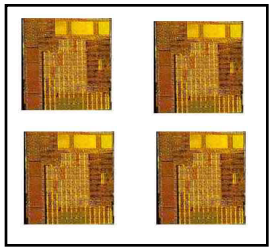
SYSTEM ON A CHIP



PowerPC 620
5 • 10^6 Transistors

From Subsystems to Macro-Cells





Programmable
macro-cells
on a single chip

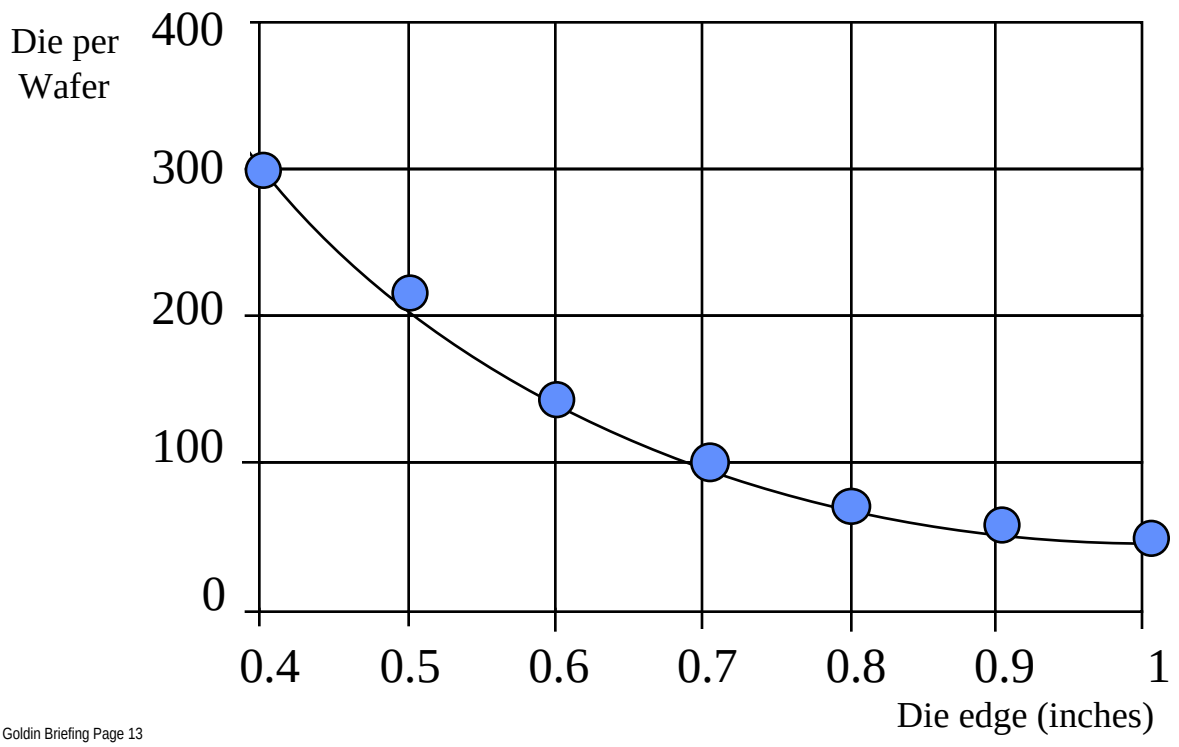
- CAD Synthesis of Spacecraft “System”
- Integration and test has a new meaning
- Spacecraft cabling is replaced by sub-micron metal interconnect
- How many Spacecraft can fit on one wafer?

New Millennium Program Office
Microelectronics Systems

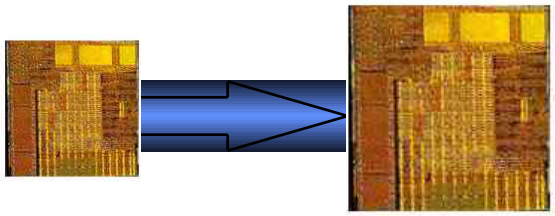
N M P

How Many Spacecrafts on a Wafer?

Possible Die from 8” Wafer



Increasing functional density while reducing cost per function.

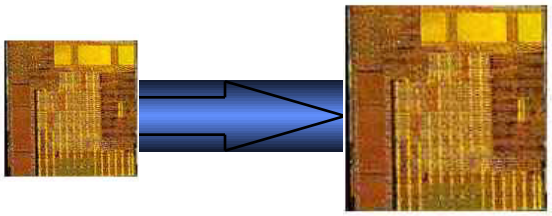


gen. x **gen. x + 1**

The basis for the sustained growth of the semiconductor industry is the exponential growth of functional density and the 30% per year, per function reduction in cost due to:

- Design innovation
- Device shrinkage
- Wafer size increase
- Die size increase
- Yield improvement
- Improvement in capital equipment utilization

The semiconductor industry yield is at an all-time high!



gen. x **gen. x + 1**

Electrical Defect Density

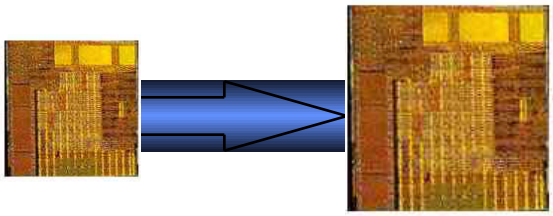
Year	’95	’98	’01	’04	’07	’10
Feature Size (µm)	0.35	0.25	0.18	0.13	0.10	0.07
d/m^2	240	160	140	120	100	25

Source: SIA ’95

Yield ≥ 90%

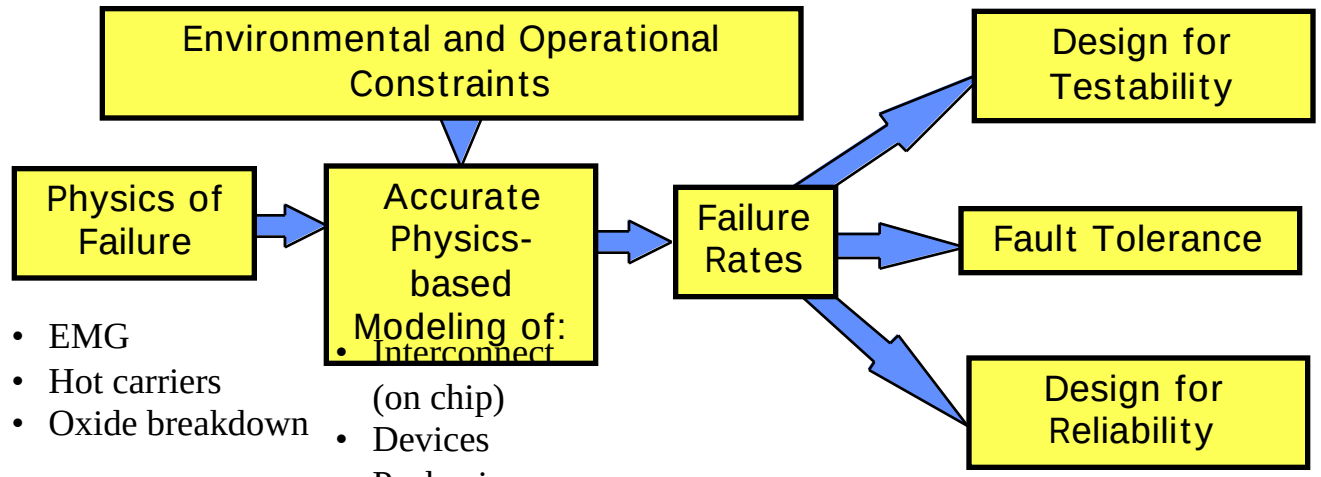
[d/m^2] is a mathematical model based on statistical evidence of those defects that cause a chip to electrically fail. It is independent of chip size.

Improving functional reliability.



gen. x **gen. x + 1**

New Millennium Program Office
Microelectronics Systems



- EMG
- Hot carriers
- Oxide breakdown

- Interconnect (on chip)
- Devices
- Packaging

- Current densities
- Geometry
- Materials
- Void, crack growth
- Stress Distribution

New Millennium Program Office
Microelectronics Systems

Integrated Product Development Team Technology Roadmap

New Millennium Program Office
Microelectronics Systems

Key Capability Needs for the 21st Century

- Develop reduction of all spacecraft electronics mass, volume and power by two orders of magnitude relative to the state-of-the art in space flight computing
- Accelerated insertion of commercial technology, components, and processes into space flight applications for the reduction of the total spacecraft life-cycle cost
- Scaleable and fault-tolerant on-board computing architectures that will enable autonomous spacecraft control and operation, and on-board science data analysis, for the the purpose of reducing the total system cost, and increase the mission scientific return.

New Millennium Program Office
Microelectronics Systems

Candidate High-Priority Technologies

- Highly integrated and modular 3D avionics architectures amenable to industry standardization
- Integrated power management electronics
- Advanced microelectronics packaging technologies such as Multichip Modules (MCMs), 3d chip stacking, and MCM stacking
- Low power electronics
- High-density low-power data storage technology
- High-bandwidth low-power interfaces
- Scaleable on-board real-time and reliable multiprocessing
- Fault tolerant computing
- Techniques for rapid prototyping

New Millennium Program Office
Microelectronics Systems

Industry Roadmap Team

Technology Area	Members
Semiconductors	MIT/LL - Craig Keast Loral - Bob Delean
Processors	Loral - Bob Delean AFPL - Captain Ronald Marx (LM) - Gerhard Franz
Storage	Honeywell - John Samson TRW - Darby Lee tarry
I/O	TRW - Darby Lee Terry Optivision - Robert Kalman Boeing - Warren Snapp
Packaging	LM - Gerhard Franz SCC - Nicholas Tenenketges UCSD - Volkan Ozguz GIT - Abhijit Chatterjee
Power	LM - Gerhard Franz Boeing - Warren Snapp
Design Automation	USC - Massoud Pedram GIT - Abhijit Chatterjee

New Millennium Program Office
Microelectronics Systems

N M P

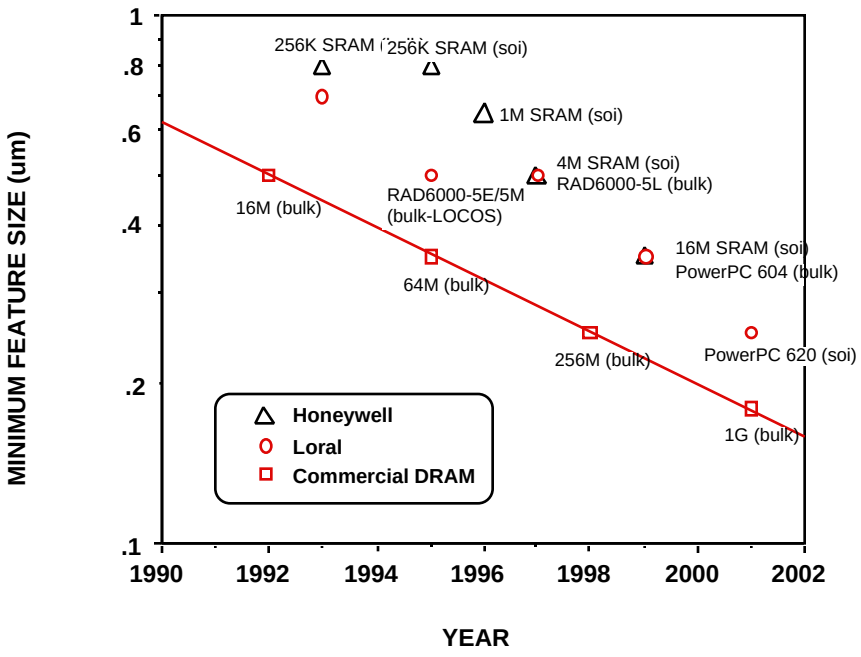
SEMICONDUCTOR INDUSTRY ASSOCIATION ROADMAP

YEAR OF FIRST DRAM SHIPMENT	1995	1998	2001	2004	2007	2010
MINIMUM FEATURE (µm)	0.35	0.25	0.18	0.13	0.10	0.07
Memory						
Bits/Chip (DRAM/Flash)	64M	256M	1G	4G	16G	64G
Cost/Bit @ volume (millicents)	0.017	0.007	0.003	0.001	0.0005	0.0002
Logic (High Volume: Microprocessor)						
Locig Transistors/cm^2 (packed)	4M	7M	13M	25M	50M	90M
Bits/cm^2 (cache SRAM)	2M	6M	20M	50M	100M	300M
Cost/Transistor @ volume (millicents)	1	0.5	0.2	0.1	0.05	0.02
Logic (Low Volume: ASIC)						
Transistors/cm^2 (auto layout)	2M	4M	7M	12M	25M	40M
Non-recurring engineering cost/transistor (milicents)	0.3	0.1	0.05	0.03	0.02	0.01
Chip Frequency (MHz)						
On-chip clock, cost-performance	150	200	300	400	500	625
On-chip clock, high-performance	300	450	600	800	1000	1100
Chip-to-board speed, high performance	150	200	250	300	375	475
Chip Size (mm^2)						
DRAM	190	280	420	640	960	1400
Microprocessor	250	300	360	430	520	620
ASIC	450	660	750	900	1100	1400
Power Supply Voltage (V)						
Desktop	3.3	2.5	1.8	1.5	1.2	0.9
Battery	2..5	1.8 - 2.5	0.9 - 1.8	0.9	0.9	0.9

New Millennium Program Office
Microelectronics Systems

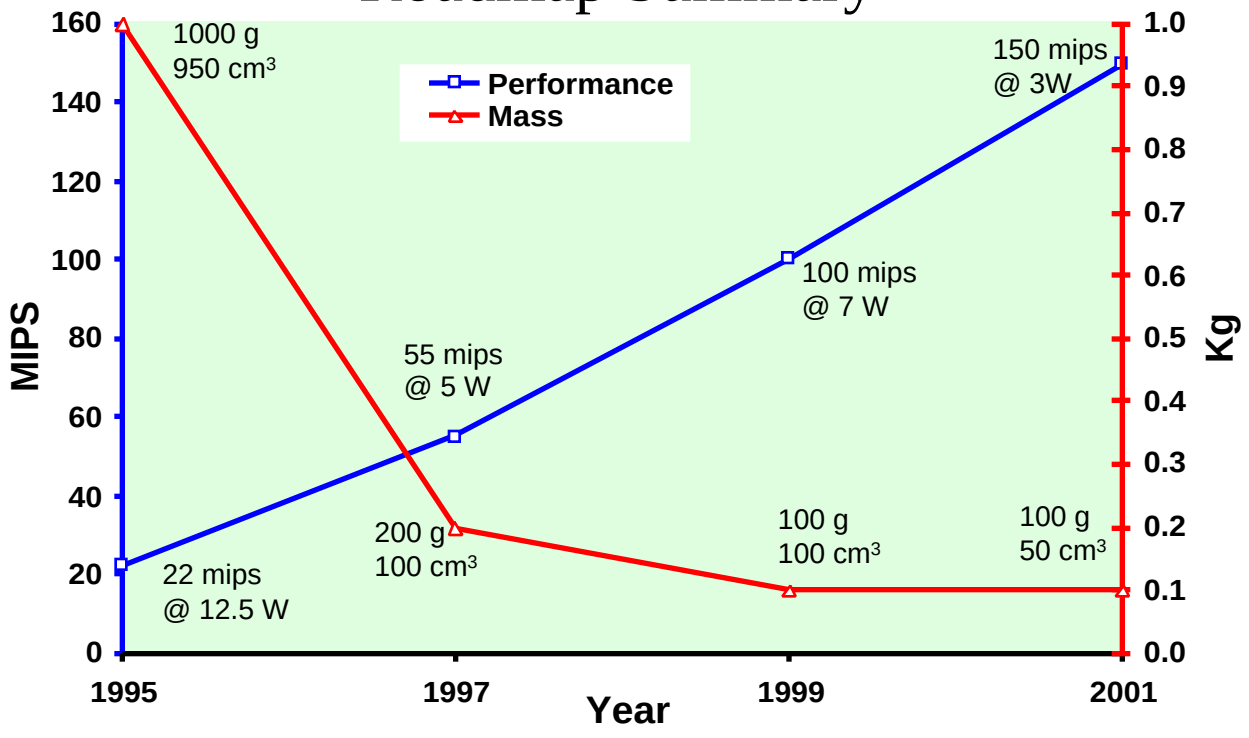
Microelectronics Feature Size

SPACE COMPONENT MINIMUM FEATURE SIZE SEMICONDUCTOR ROADMAP



New Millennium Program Office
Microelectronics Systems

General Purpose Processor Roadmap Summary

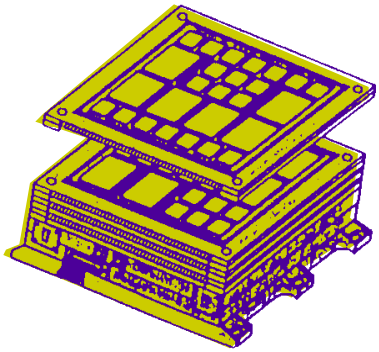


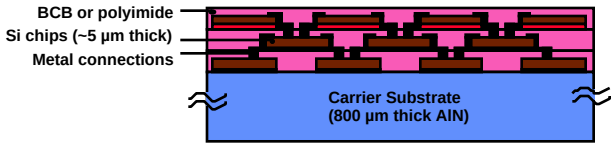
New Millennium Program Office
Microelectronics Systems

Packaging Roadmap Summary

- Vision: Towards 3D VLSI
- Metrics: level of integration, size, mass, power density.
- Roadmap:

	Low-cost 3D MCM + HDI	3D HDI	3D VLSI
	97	99	01
Integration	medium	high	very high
Volume (cc) (dgtl+pwr)	600+1000	400+500	70+100
Mass (g) (dgtl+pwr)	1000+2000	500+500	300+300
• Capabilities	Some HDI	3D HDI	3D HDI
	Mixed MCM	3D VLSI	3D VLSI
	MCM/SMT	3D Stack PCBs	3D MCM
	3D Stack PCBs		





New Millennium Program Office
Microelectronics Systems

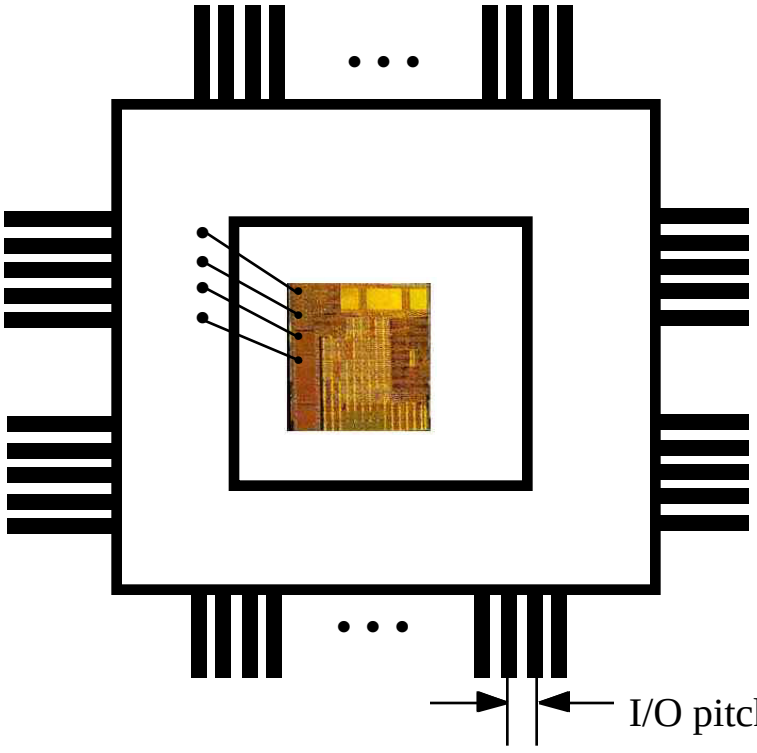
3D VLSI Technology Development

- Eliminating the Single Chip Package Bottleneck

New Millennium Program Office
Microelectronics Systems

N M P

Single Chip Package I/O Bottleneck



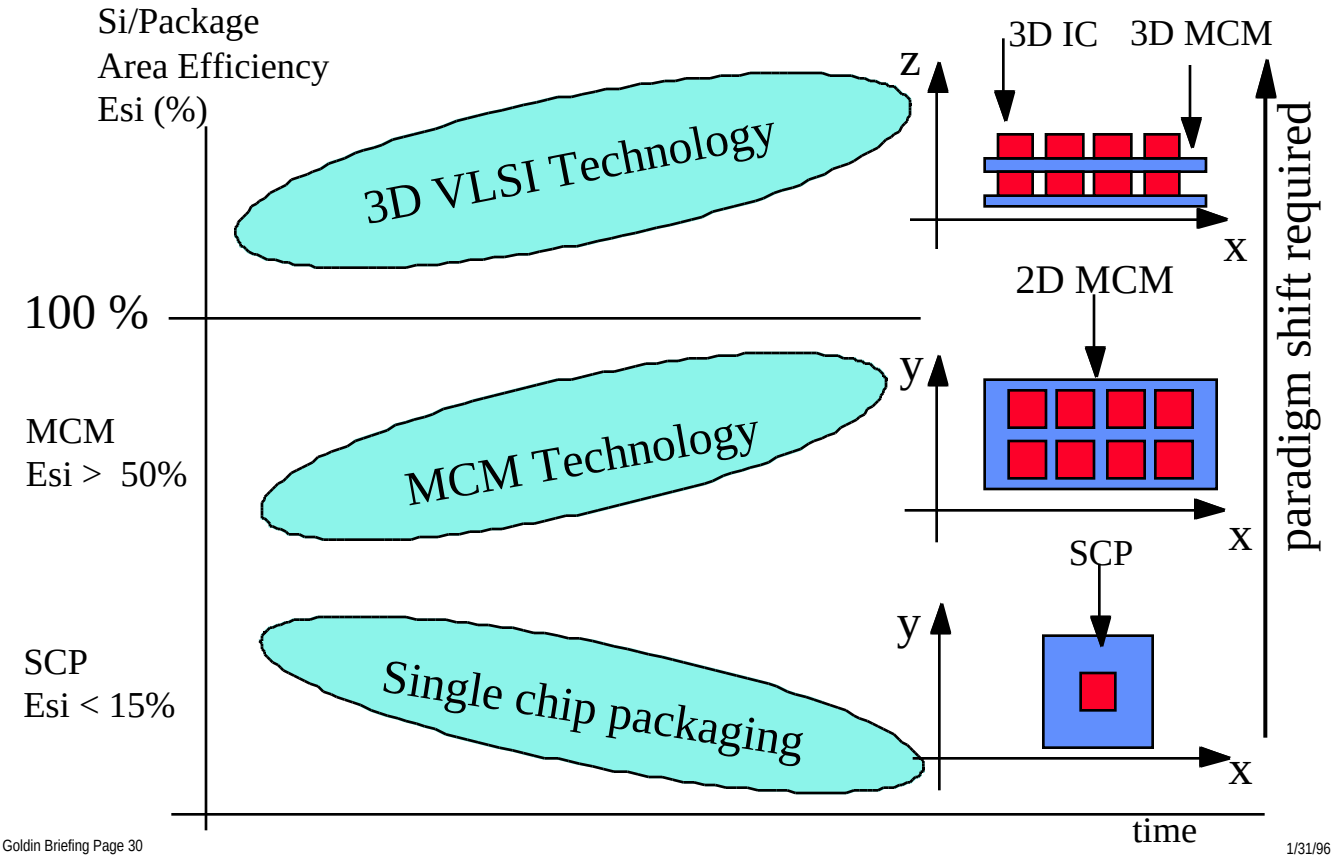
I/O pitch: ~ 1-2 mm

	through-hole	surface mount
I/O pitch:	~ 1-2 mm	0.5-1 mm

VLSI Chip Evolution:

- Feature size reduction
- Chip size growth
- Chip speed growth
- Chip I/O count growth

New Millennium Program Office
Microelectronics Systems



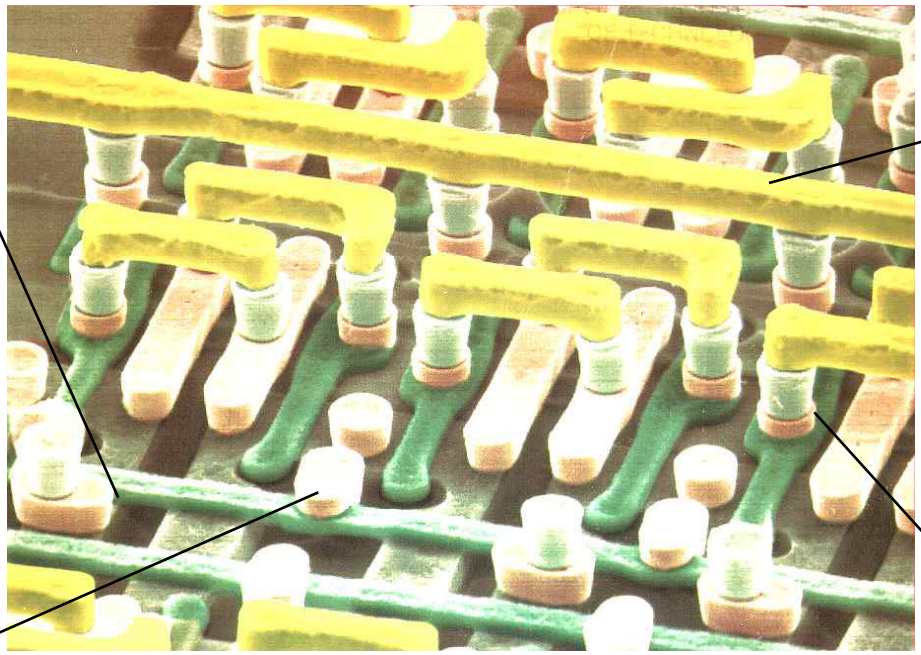
1/31/96

New Millennium Program Office
Microelectronics Systems

N M P

SRAM Array Interconnect

Green
Word lines (polysilicon)



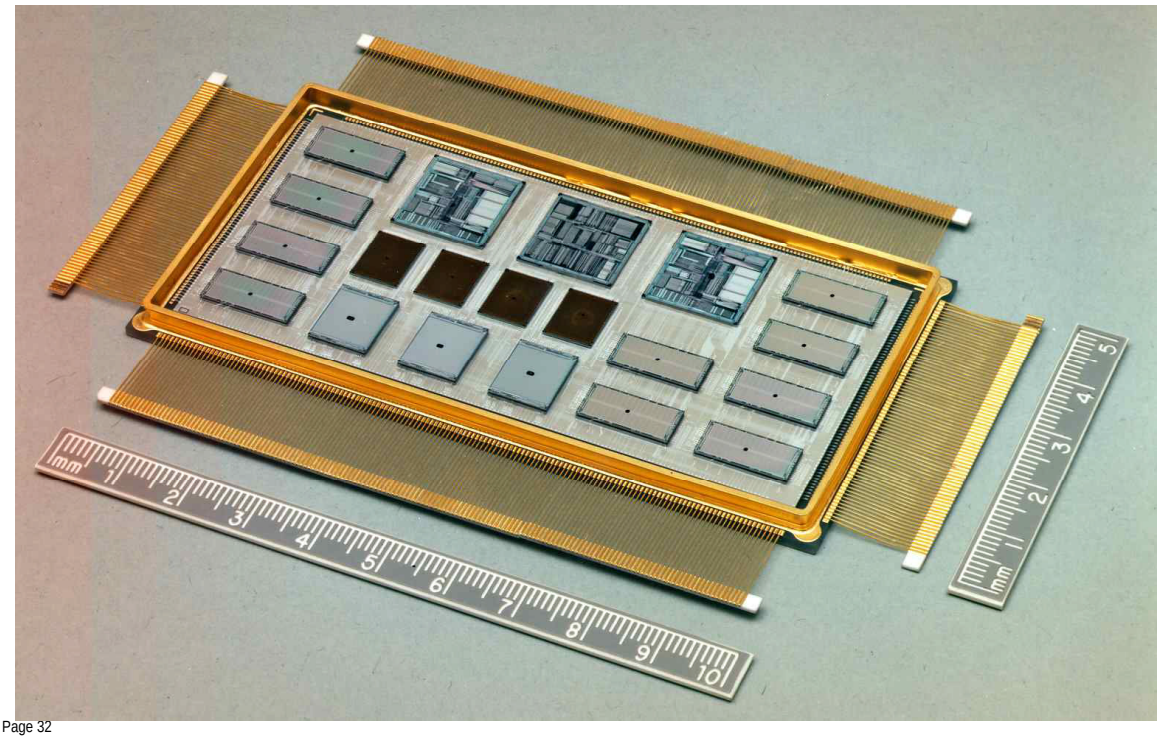
Yellow
Global interconnect (TiAl (cu) Ti/TiN)

Pink
Local interconnect for n^+, p^+ (tungsten) diffusion contacts

Light Green
Contact Studs to global interconnect (tungsten)

New Millennium Program Office
Microelectronics Systems

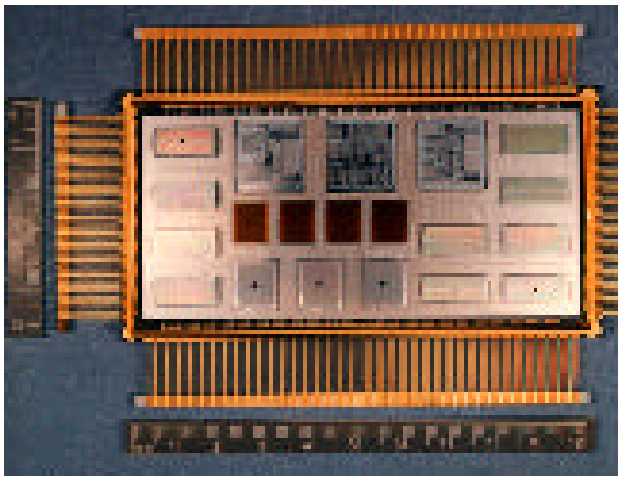
NASA's Advanced Flight Computer
33-Chip Multichip Module



New Millennium Program Office
Microelectronics Systems

NASA's 33-Chip Flight Computer Module

- Flight Computer System integrated into a single MCM of 33 chips.
- 3D IC stacking used for SRAM and EEPROM memory.
- Si Substrate for inter-chip connections.
- MCM-D Al metal and SiO2 dielectric.
- Mass < 100 grams (89 grams)
- Volume < 1.5 ci
- AlN 442 leaded package
- Rad-hard, R3000 ISA, TRW RH-32
- 20 MIPS @ 25 MHz and < 12 watts
- Industry partnership: TRW, nCHIP.
- Flight validation on SSSTI 7/96.



New Millennium Program Office
Microelectronics Systems

N M P

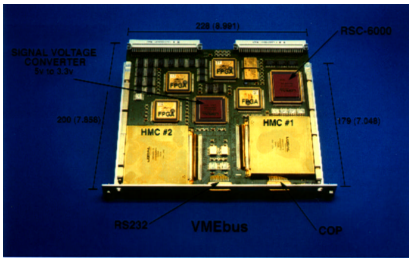
10 Kg

Mass

1 Kg

100 g

Cassini Flight Computer

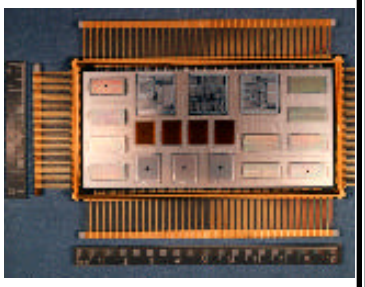


Mars Pathfinder
Flight Computer*

* Mars Pathfinder Flight Computer
10 x greater performance
than Cassini Flight Computer

* Equal Performance
to Mars Pathfinder
Flight Computer

Advanced Flight
Computer*



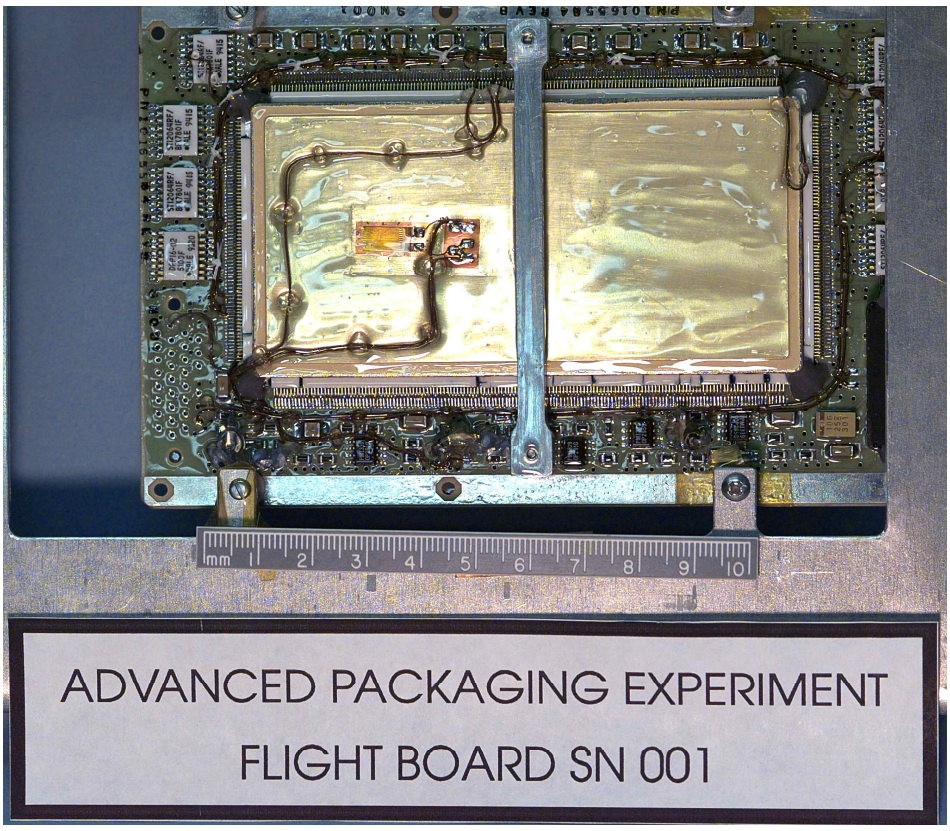
1980'S

1990'S

NEW MILLENNIUM

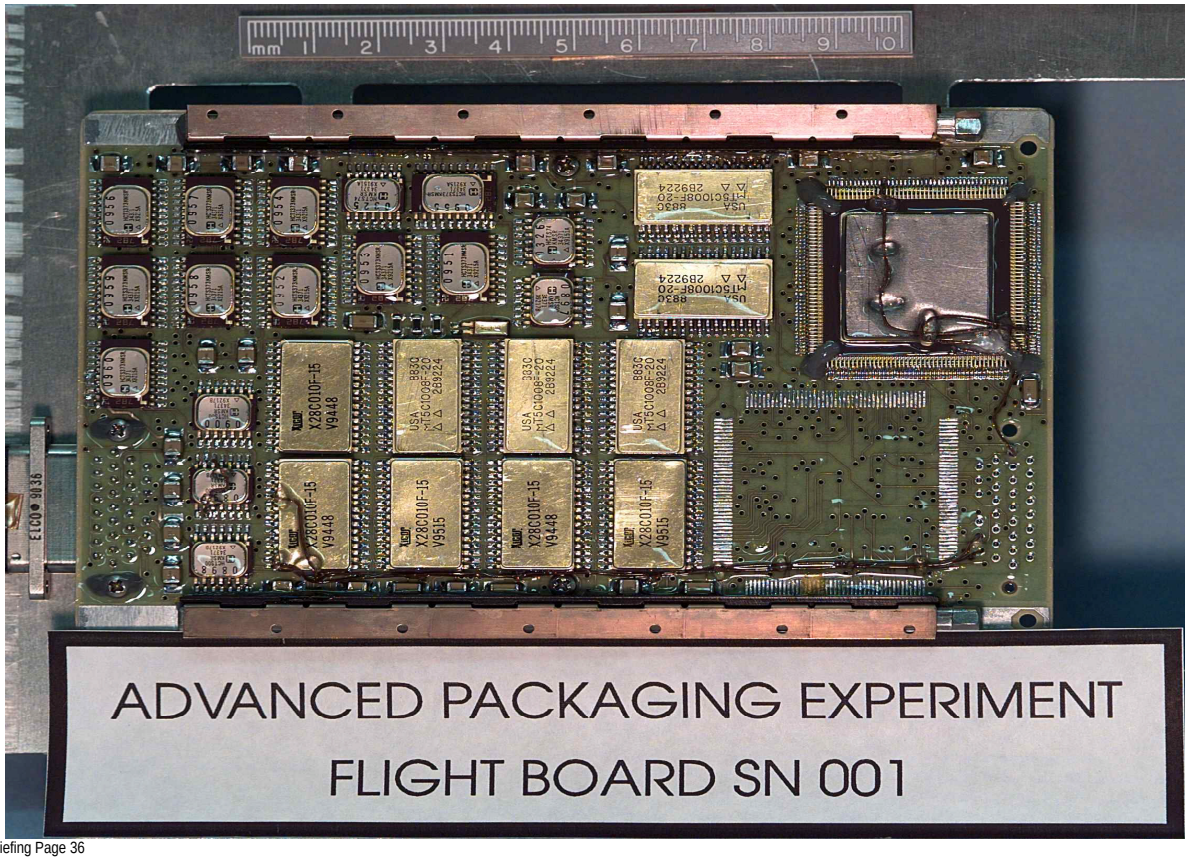
New Millennium Program Office
Microelectronics Systems

Advanced Flight Computing Program



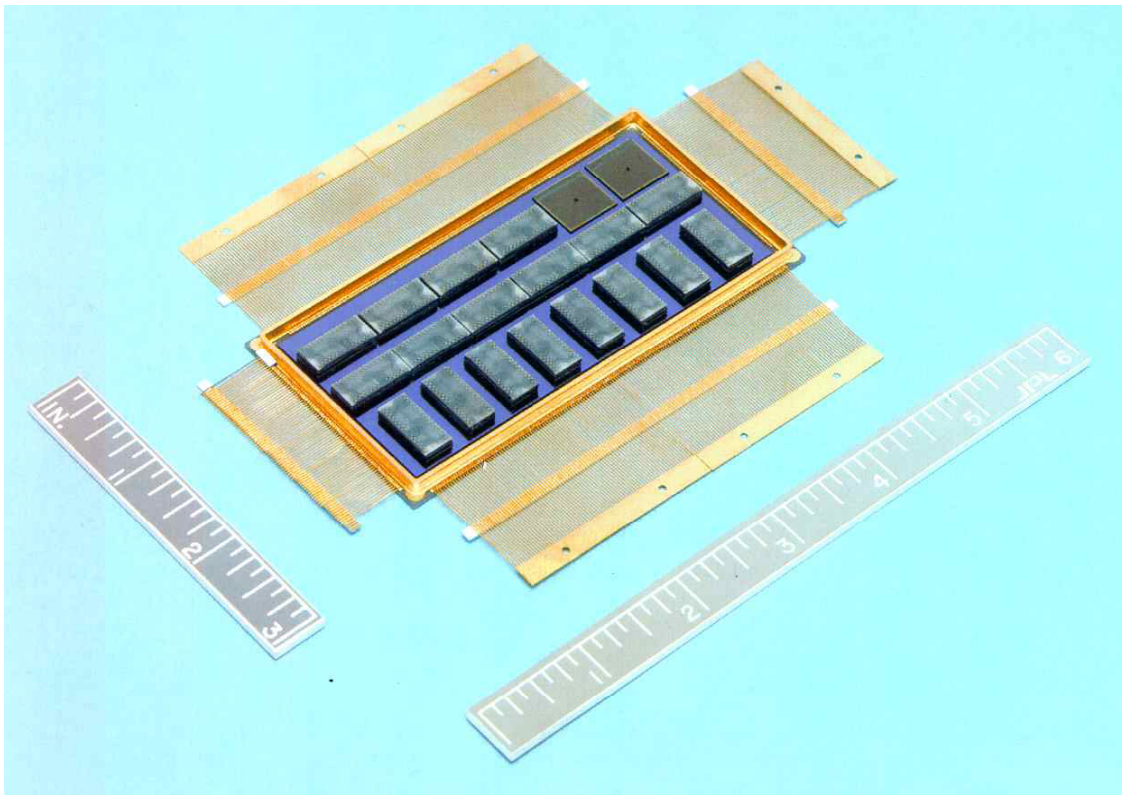
New Millennium Program Office
Microelectronics Systems

Advanced Flight Computing Program

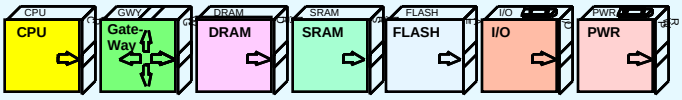


New Millennium Program Office
Microelectronics Systems

NASA's AFC Mass Memory Module

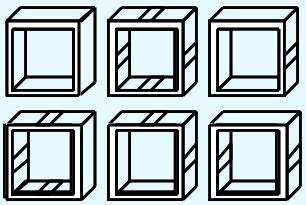


SPACE-CUBE ARCHITECTURE

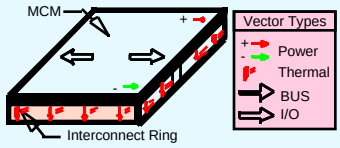


Available Flavors

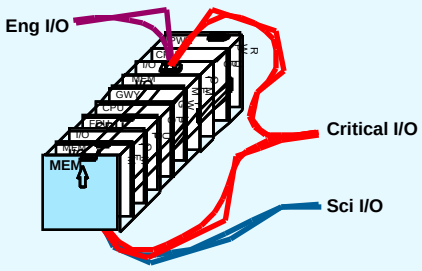
and others • • •



Interconnect Rings



Module Abstraction



Spacecraft Example
(Pluto Express Architecture)

FEATURES

- Processor Independent
- Interchangeable Modules
- Maintainable & Upgradeable
- Standard Features
  - Module Size & Shape
  - Interconnect Bus
  - Interconnect Method
- Can Be Easily Configured To The Following Architectures
  - Single String
  - Dual String
  - TMR
  - Multiprocessors
  - Distributed
  - NonDistributed
  - Others
- Module Inheritance from AFC
- Modules & Interconnections Are Simplified Yet Complicated Architectures Can Be created.
- Architecture Applies Regardless Of Granularity
  - Board Level
  - Stacked MCMs
  - Stacked Dies
- Interconnections Do Not Cross

gsb 3/25/95

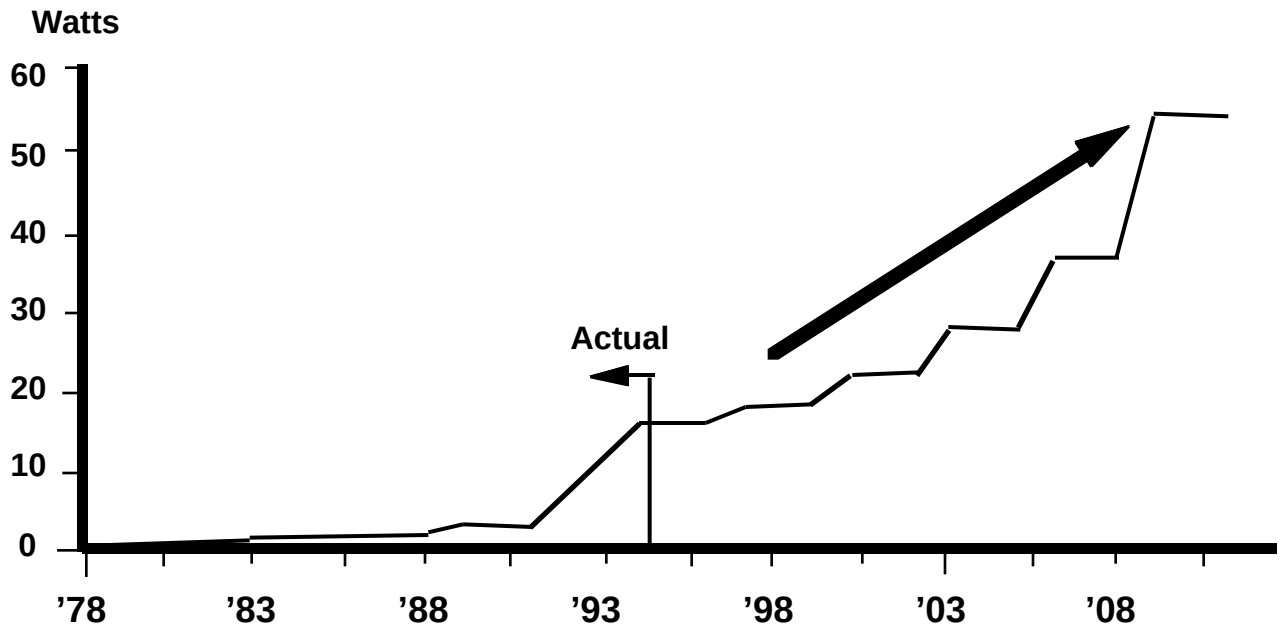
New Millennium Program Office
Microelectronics Systems

Low-Power Electronics Technology Development

New Millennium Program Office
Microelectronics Systems

N M P

Power Consumption



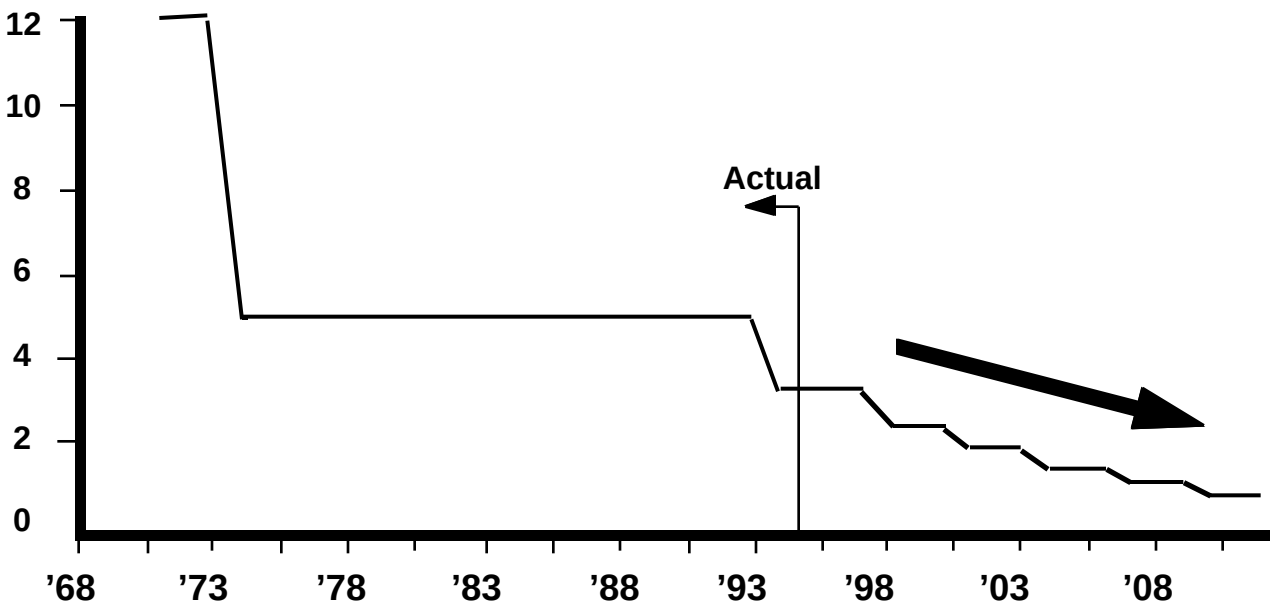
Source: Intel, SIA Technology Roadmap

Key Drivers for Voltage Scaling

- Reduced Power dissipation, P:
  $P = f \cdot c \cdot v^2 \cdot \alpha$
- Higher Reliability
- Reduced Transistor Channel length
- Extended Battery Lifetime

New Millennium Program Office
Microelectronics Systems

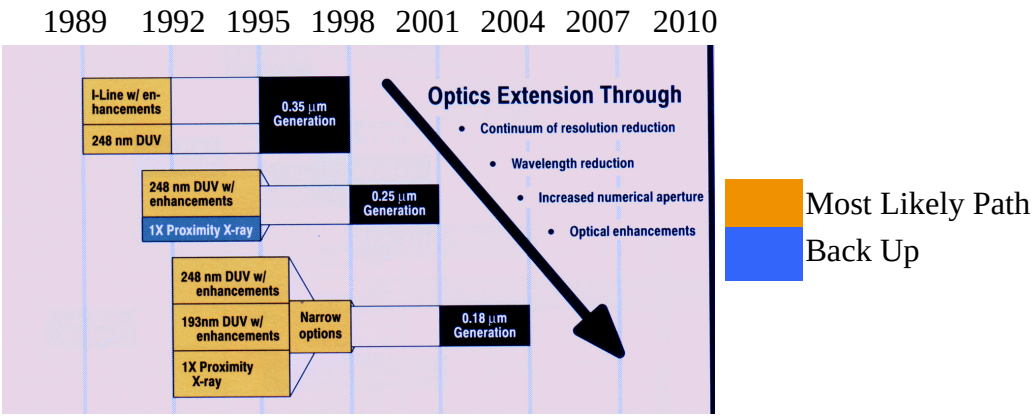
Voltage Scaling



Source: Intel, SIA Technology Roadmap

New Millennium Program Office
Microelectronics Systems

Advanced Optical Lithography Roadmap



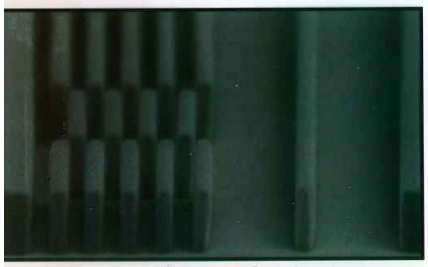
- MIT Lincoln Laboratory has production worthy i-line and 248 nm DUV wafer steppers, as well as the world's only 193 nm DUV wafer step and scan system. All three tools are operating in Lincoln's class-10 semiconductor fabrication facility, allowing future deep-submicrometer technologies to be investigated today.
- This advanced optical lithography capability is currently being used to develop a sub 0.25 µm low power (V_{DD} = 0.9 V) SOI CMOS process technology suitable for a wide range of low power, high performance applications.

193-nm PROJECTION LITHOGRAPHY

193-nm LITHOGRAPHY SYSTEM

LINCOLN LABORATORY 193-nm EXPOSURE SYSTEM

- SPECIFICATIONS
  - ArF EXCIMER LASER SOURCE
  - 0.5 NA OPTICS
  - 4x REDUCTION PRINTING
  - 22 x 32.5 mm EXPOSURE FIELD
  - BASED ON SVGL MICRASCAN II STEP AND SCAN
- RESOLUTION
  - 0.18 TO 0.25 μm WITH CONVENTIONAL PHOTOMASK
  - 0.10 μm WITH PHASE-SHIFT PHOTOMASK
- STATUS
  - INSTALLED IN MICROELECTRONICS LABORATORY
  - HIGH RESOLUTION ACHIEVED OVER FULL FIELD
  - OFF-AXIS ALIGNMENT INSTALLED
  - AUTOMATIC WAFER HANDLING SYSTEM INSTALLED
  - BEING QUALIFIED JOINTLY WITH INDUSTRY



0.20 μm FEATURES

ISOLATED LINES

New Millennium Program Office
Microelectronics Systems

N M P

SILICON-ON-INSULATOR TECHNOLOGY FOR LOW POWER ELECTRONICS

PROGRAM HIGHLIGHTS:

UTILIZES WORLD'S MOST ADVANCED OPTICAL LITHOGRAPHY TECHNOLOGY.
- INITIAL WORK USING 248-nm LITHOGRAPHY WITH TRANSFER TO 193-nm LITHOGRAPHY

LOW POWER OPERATION, 1 VOLT SUPPLY, 0.3 VOLT THRESHOLDS.

FULLY-DEPLETED DEVICE DESIGN FOR REDUCED PARASITIC CAPACITANCES AND NEAR IDEAL SUBTHRESHOLD SLOPES.

PROCESS HIGHLIGHTS:

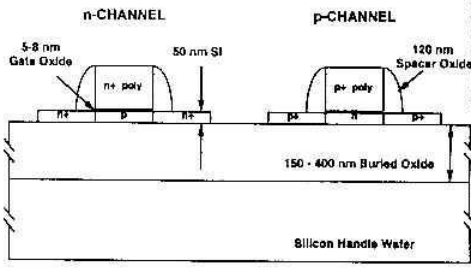
50 nm ACTIVE SILICON THICKNESS WITH COMPLETE OXIDE ISOLATION.

DUAL-DOPED POLY FOR COMPLIMENTARY THRESHOLD MATCHING.

SELF-ALIGNED SHALLOW SILICIDE PROCESS WITH OXIDE SPACERS.

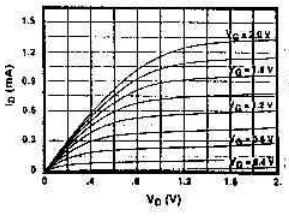
ALUMINUM REFLOW CONTACT FILL TECHNOLOGY.

FULLY-DEPLETED, < 0.25 µm, SOI CMOS

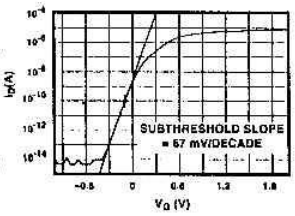


n-CHANNEL TRANSISTOR CHARACTERISTICS
(W/L = 6 µm/0.25 µm)

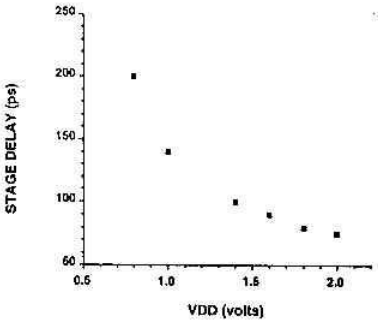
DRAIN CURRENT vs DRAIN VOLTAGE



DRAIN CURRENT vs GATE VOLTAGE



0.25 um RING OSCILLATOR STAGE DELAY



Low Power Electronics Development Approach:

- Collaborate with ARPA on the ULPE Program
- Work with Industry: Intel, IBM, Motorola
- Work with Academia: USC, GIT, Stanford
- Work with other National Labs: MIT/LL, SNL
- Fly LPE Experiment on DS1:
  0.18µ SOI, 1 volt technology
- Initiate LPE R&D task at JPL in FY 96

New Millennium Program Office
Microelectronics Systems

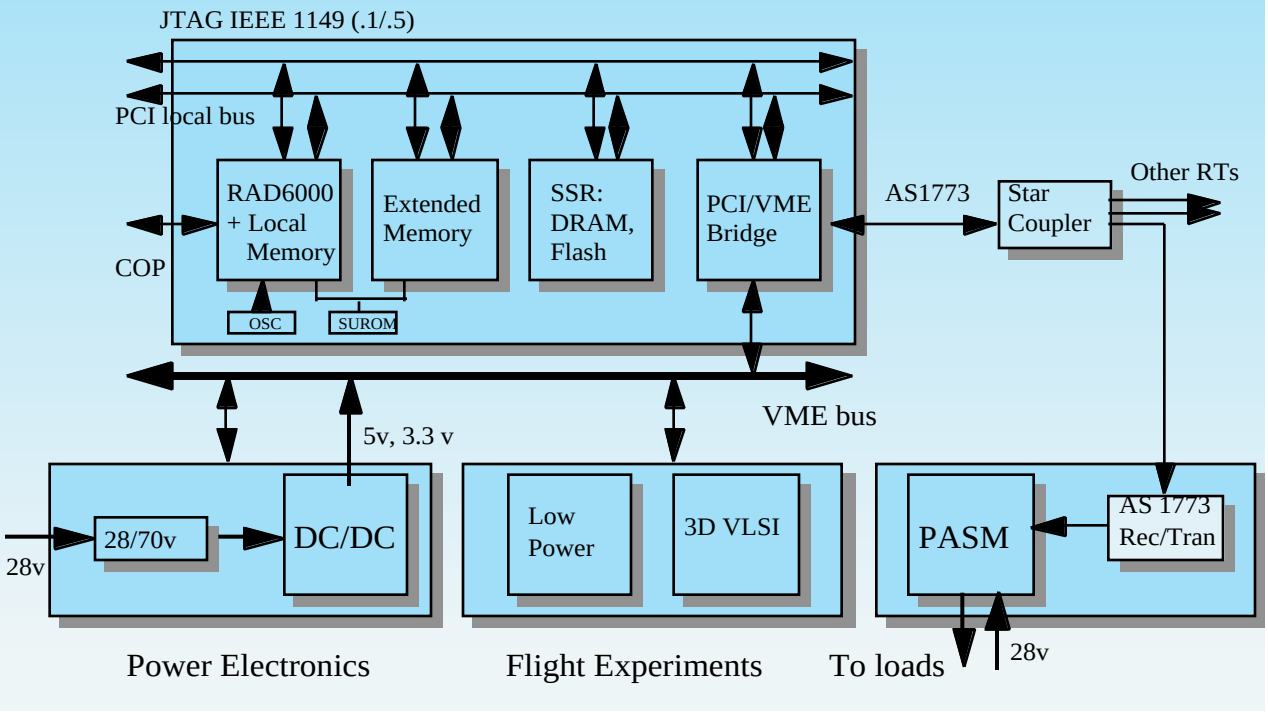
Low Power Electronics R&D at JPL

- LPE Library Development
- Circuit Design, Simulation, and Test
- Radiation Test and Analysis
- Physics of Failure Analysis
- Reliability modeling and Analysis
- Low-Power Opto-Electronics Development with Optivision (SBIRs 1 and 2), for Low-Power 1773 s/c bus
- Low-Power Systems Design
- Low-Power Design Synthesis

New Millennium Program Office
Microelectronics Systems

Deep-Space 1 Avionics Architecture

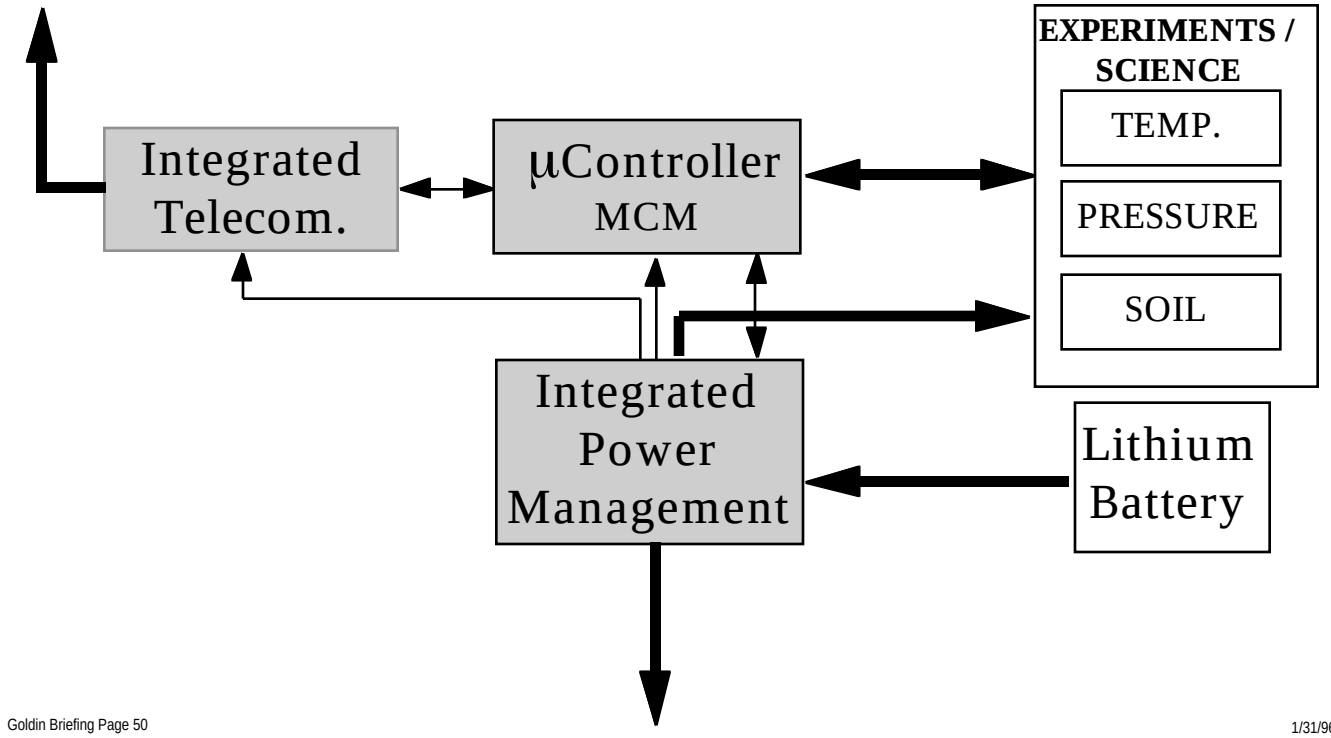
DS1 Target Architecture



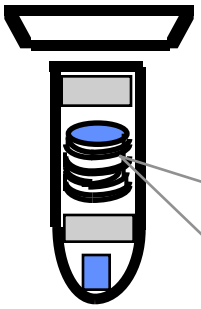
New Millennium Program Office
Microelectronics Systems

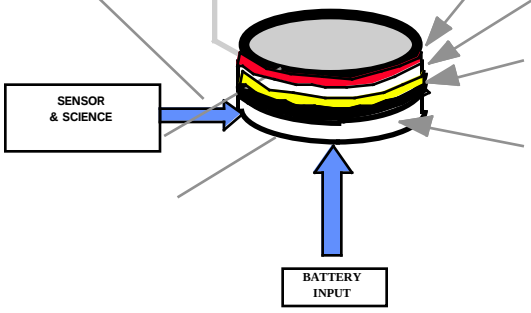
N M P

DS2 Target Architecture



3D High Density Interconnected Avionics Stack





- Integrated Telecommunication
- Instrument Electronics
- mController MCM
- Integrated Power Management

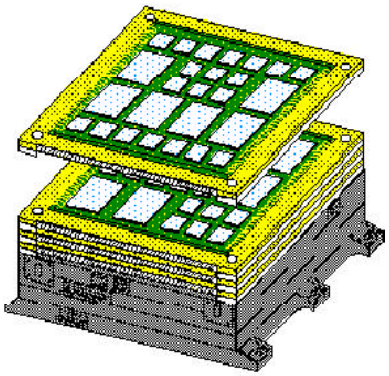
New Millennium Program Office
Microelectronics Systems

Customers and Partnerships

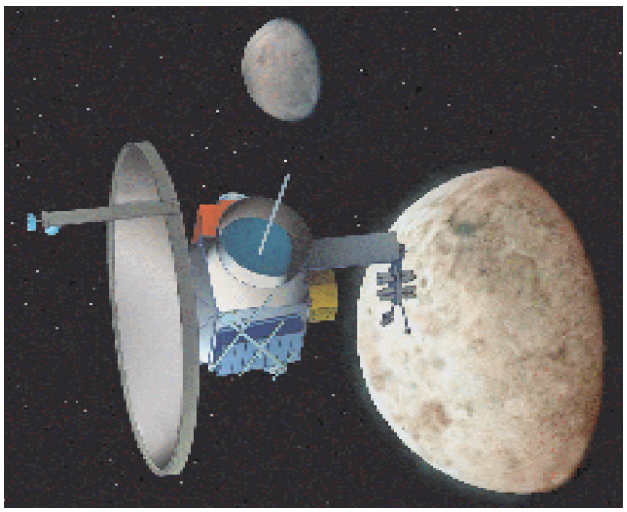
New Millennium Program Office
Microelectronics Systems

N M P

Pluto Express

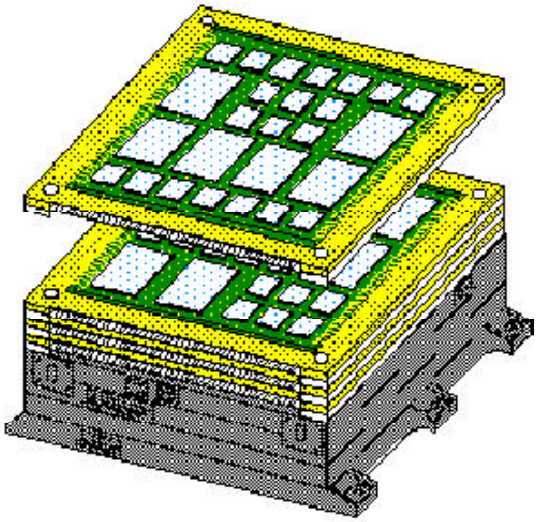


- **Reliability**
- **Low Power**
- **Fault Tolerance**
- **Miniaturization**



New Millennium Program Office
Microelectronics Systems

Advanced Avionics Technology for Reusable Launch Vehicles



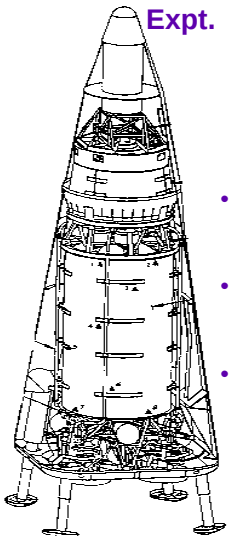
Reliability

Test and Maintenance

Fault Tolerance

Miniaturization

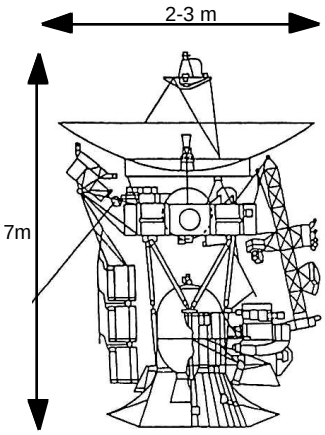
RI & MD
DC-XA LH2 Tank Expt.



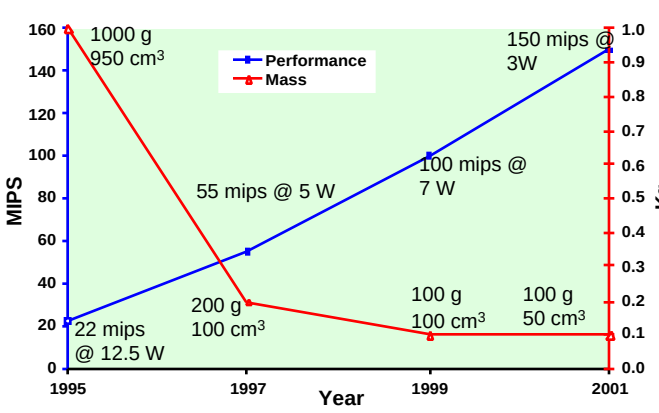
- **Passive AU & AE sensors (60-500 KHz)**
- **Acoustic environment 150-170dB**
- **Severe cryoshock & vibration exposure**

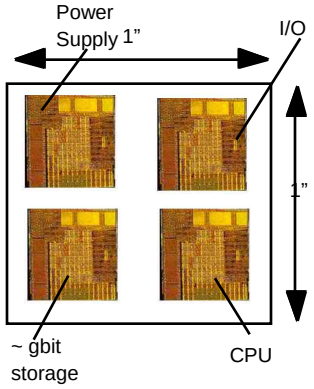
New Millennium Program Office
Microelectronics Systems

Vision: A Spacecraft on a Chip



VOYAGER
1976
~# transistors





ystem on a Chip
“New Millenniumm”
5 * 10^6 transistors
today

- **Exponential Growth of Functional Density while reducing cost per function**
- **Design Automation Synthesis**
- **System on a Chip**